IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

TELCORDIA TECHNOLOGIES, INC.,	)	
	)	
Plaintiff/Counterclaim Defendant,	)	
	)	C.A. No. 04-876-GMS
v.	)	
	)	
CISCO SYSTEMS, INC.,	)	
	)	
Defendant/Counterclaim Plaintiff.	)	

TELCORDIA'S ANSWERING BRIEF IN OPPOSITION TO
CISCO'S MOTION FOR JUDGMENT AS A MATTER OF LAW

ASHBY & GEDDES
Steven J. Balick (I.D. #2114)
John G. Day (I.D. #2403)
Tiffany Geyer Lydon (I.D. #3950)
500 Delaware Avenue, 8th Floor
P.O. Box 1150
Wilmington, DE 19899
(302) 654-1888

Attorneys for Plaintiff
Telcordia Technologies, Inc.

Of Counsel:

Donald R. Dunner
Steven M. Anzalone
Richard H. Smith
Vincent P. Kovalick
Laura P. Masurovsky
James T. Wilson
John M. Williamson
FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.
901 New York Ave., N.W.
Washington, D.C. 20001
(202) 408-4000

Dated: July 23, 2007

TABLE OF CONTENTS

TABLE OF AUTHORITIES

CASES

STATUTES

I. Introduction

On May 11, 2007, the jury in this case found that Cisco willfully infringed Telcordia's '763 and '633 patents and that Telcordia's '763, '633, and '306 patents were not invalid and were enforceable. Substantial evidence unquestionably supports the jury's verdict on all issues. Nevertheless, Cisco renewed its motions for judgment as a matter of law, contending that no reasonable juror could find (1) that the '763 patent is infringed, (2) that the claims of the '763 patent are not indefinite, (3) that the '633 patent is not invalid, and (4) that the '306 patent is not invalid. In an effort to support its renewed JMOL motions, Cisco grossly mischaracterizes the record in this case, repeatedly and incorrectly suggesting that Telcordia conceded, admitted, or failed to respond to the key, hotly contested issues in the case. Telcordia did not simply admit, concede, or fail to respond to any key issue in the case. To the contrary, for each issue Telcordia presented substantial evidence upon which the jury properly based its verdict.

II. Legal Standard

A post-verdict motion for JMOL "should be granted only where there is no legally sufficient basis for a reasonable jury to have found for the non-moving party." *Price v. Delaware Dept. of Correction*, 40 F. Supp.2d 544, 549 (D. Del. 1999) *citing Garrison v. Mollers N. Am., Inc.*, 820 F. Supp. 814, 818-19 (D. Del. 1993). In reviewing a renewed JMOL motion, the court must "consider the evidence in the light most favorable to the nonmoving party and afford the nonmoving party the benefit of all logical inferences." *Boyce v. Edis Co.*, 224 F. Supp.2d 814, 816 (D. Del. 2002) *citing Keith v. Truck Stops Corp. of Am.*, 909 F.2d 743 (3d Cir. 1990). "The movant has a difficult burden." *Id.* at 816. If the "record contains the minimum quantum of evidence from which a jury might reasonably afford relief" then the reviewing court

must deny the motion. *Keith,* 909 F.2d at 745 *quoting Smollett v. Skayting Dev. Corp.*, 793 F.2d 547 (3d Cir. 1986).[1]

III. The '763 Patent

A. Substantial Evidence Supports the Jury's Finding of Infringement of the '763 Patent

Having been properly instructed on the meaning of the '763 claim terms as determined by the Court in its June 22, 2006, Claim Construction Order, the jury found that Cisco willfully infringed Telcordia's '763 patent covering UPSR technology. Cisco now contends that no reasonable jury could have found that Cisco's products meet the limitation "inserting an error signal on designated ones of said [the] subrate communications," which the Court construed to require "inserting an error signal on the channels ***following demultiplexing***." D.I. 179 at ¶ 5; D.I. 376 at 2-12. But the jury's finding that Cisco's products meet the "following demultiplexing" limitation is unquestionably supported by substantial evidence.

During trial, Telcordia presented ample evidence establishing that Cisco's ONS products—those which the jury determined infringed Telcordia's '763 patent—perform the following operations in the following order:

(1) **first insert line error signals** (AIS-L signals) at the receive framer (*see, e.g.*, Trial Tr. 1072 (Dr. Prucnal));

(2) **then demultiplex at the pointer processor component** (*see, e.g.*, Trial Tr. 1064-1066 (Dr. Prucnal describing demultiplexing at the "pointer interpreter" portion of the pointer processor));

[1] The Federal Circuit applies the law of the regional circuit as to the legal standard for deciding JMOL motions. *See, e.g., Pharmastem Therapeutics, Inc. v. Viacell, Inc.*, Nos. 05-1490, 05-1551 (Fed. Cir. July 9, 2007)("Under Third Circuit law, which in this case dictates the standard for reviewing the denial of the motion for JMOL, we review the district court's action '*de novo* by reapplying the JMOL standard' applied by the district court.").

(3) **then insert path error signals** (AIS-P signals) at the pointer processor component (*see, e.g.*, Trial Tr. 1065 (Dr. Prucnal describing insertion of AIS-P signals at the "pointer generator" portion of the pointer processor); and

(4) **then demultiplex at the cross-connect component** (*see, e.g.*, Trial Tr. 1065, 1069, 1123 (Dr. Prucnal describing the additional demultiplexing at the cross-connect component)).

See, e.g., Trial Tr. 1064-1073 (Prucnal); PTX-388; PTX-739. As such, the evidence presented by Telcordia demonstrates that Cisco's products insert error signals (the AIS-P signals in item 3 above) following demultiplexing (the pointer processor's demultiplexing in item 2 above) as required by the Court's claim construction.

In its renewed motion for JMOL of non-infringement of the '763 patent, Cisco advances the exact same flawed arguments that it advanced—and that the Court rejected—during the summary judgment phase of the case. D.I. 376 at 4-12. Namely, Cisco ignores the evidence presented by Telcordia and contends (1) that Telcordia "conceded" that only the cross-connect (number (4) above), and not the pointer-processor (number (2) above), can be the claimed demultiplexer, and, alternatively, (2) that the Court's already narrow "following demultiplexing" construction somehow inherently includes additional limitations (never raised during claim construction) such as "following ***the ultimate*** demultiplexing" or "following demultiplexing ***but prior to insertion of any other error signals***." But Telcordia never "conceded" or "admitted" the key disputed issues in the case, and Cisco's unilateral reconstruction of the Court's "following demultiplexing" limitation has no basis in the record and is entirely inappropriate. When Cisco raised these same arguments and employed this same strategy (i.e., mischaracterizing Telcordia's contentions) during the summary judgment phase of the case, the Court rejected Cisco's position and instead concluded that

> . . . the preceding examples demonstrate that the parties' experts disagree as to whether the Pointer Processor of the defendants' accused products performs the demultiplexing and insertion of error signals required by the

> asserted claims. Moreover, Dr. Prucnal and Dr. Grover rely on the same supporting documents and deposition testimony in reaching the exact opposite conclusions with respect to the accused products. **These are not minor disagreements, but critical factual issues** that must be resolved in order to reach a finding with respect to infringement of the '763 patent. In order to resolve these disputed issues, **the factfinder will need to make credibility determinations and weigh the evidence relied on by the competing experts.**

D.I. 341 at 15 (Summary Judgment Order)(emphasis added). On the same issue (i.e., whether the "following demultiplexing" limitation is found in Cisco's products), the Court also acknowledged that "the dispute between the parties can be classified only as a classic battle of the experts." *Id.* at 13. Cisco's JMOL motion suggests that Telcordia somehow forgot to present its side of the "critical factual issues" during trial. *See, e.g.,* D.I. 376 at 4. Although ignored by Cisco, Telcordia in fact introduced substantial evidence on the "critical factual issues" regarding '763 infringement.

1. Substantial Evidence Demonstrates that the Pointer Processor Is the Demultiplexer

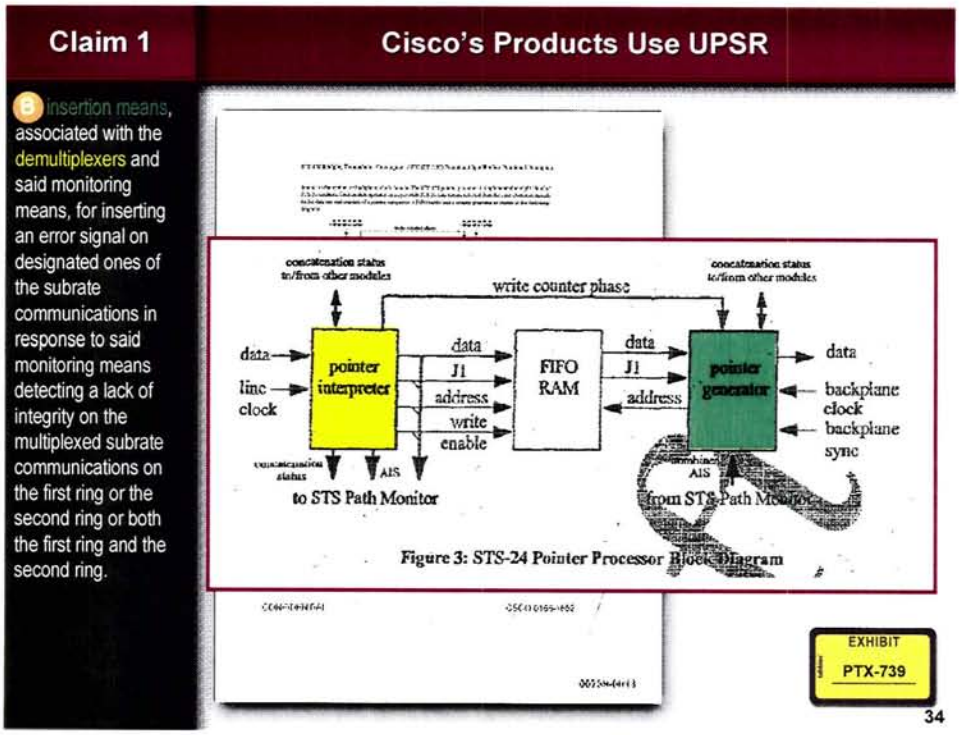
On the issue of whether the pointer processor is the demultiplexer, throughout its brief Cisco blindly and unilaterally proclaims:

- "There is no dispute that the demultiplexer is the cross-connect." D.I. 376 at 4.
- "At trial, both experts agreed that the cross-connect in Cisco's products - not the pointer processor - is the claimed demultiplexer." *Id.*
- "Dr. Prucnal conceded, as he must, that it is the cross-connect, not the pointer processor, that is the claimed demultiplexer." D.I. 376 at 5.

In other words, rather than challenging the sufficiency of the evidence that Telcordia did present to support its theory that the pointer processor is a demultiplexer as called for in the claims, Cisco simply pretends that Telcordia presented no evidence whatsoever (and even more preposterously, that Telcordia's expert actually agreed with all of Cisco's non-infringement

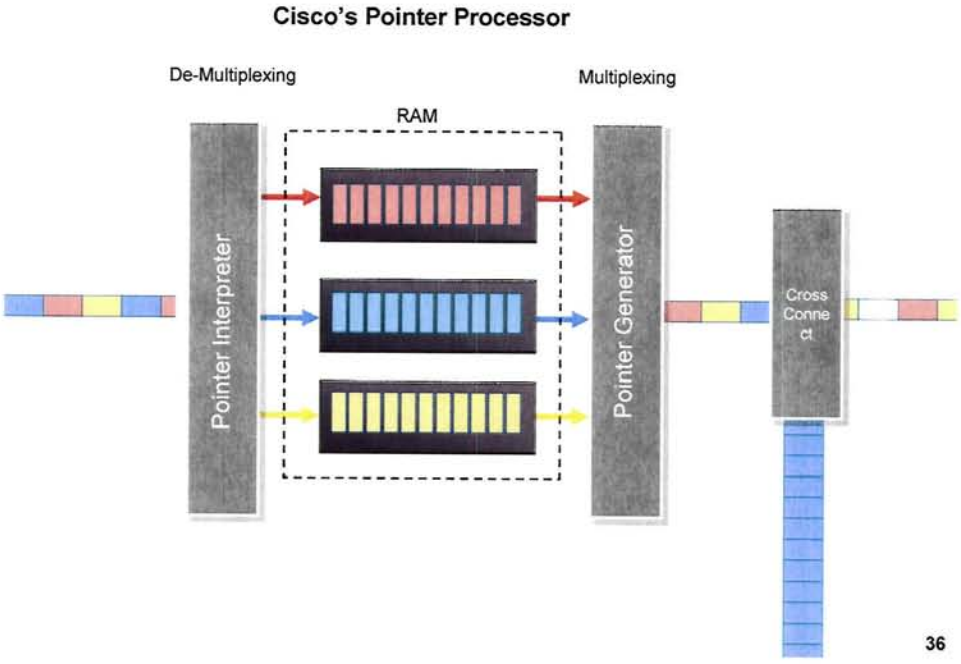
positions). Cisco employs this head-in-the-sand approach because it cannot mount any meaningful challenge to the sufficiency of Telcordia's evidence—even a cursory review of the trial record establishes ample support for Telcordia's position that the pointer processor is the demultiplexer:

- "**This [PTX-739, illustrated in Prucnal demonstrative 34 - reproduced below] is the details of what is in the pointer processor** that we've seen on the last slide. This shows what is inside and it includes data coming from the left, a pointer interpreter, something called a FIFO RAM, which is memory, and a pointer generator. The pointer generator is where the insertion of the error signal is, and the **pointer interpreter is where the demultiplexing goes on**. And so my aim is to explain and show in detail that the insertion of the error signal follows demultiplexing." Trial Tr. 1065 (Dr. Prucnal).



- "[W]hat happens is that this **pointer processor [Prucnal demonstrative 34 - reproduced above] will take apart or separate the data coming in**. Remember, I said that this data is something like an STS-3, for example. You would have to separate it into the individual STS's and it puts each of these STS's in different portions of RAM. **That is separating from a single combined data stream**

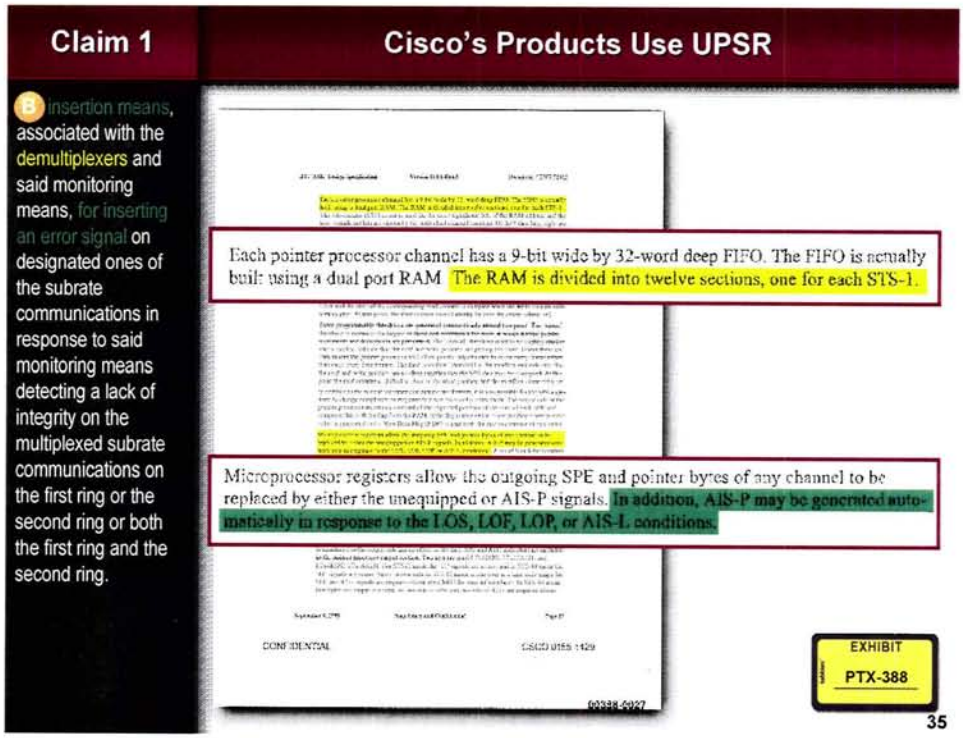
into the separate portions the STS-1s. That is called demultiplexing." Trial Tr. 1066 (Dr. Prucnal).



- "[T]his is a diagram or cartoon [Prucnal demonstrative 36 - reproduced above] of an explanation of what is going on in this pointer processor chip, so I made this up to try to illustrate what is happening. I said it several times but I think a picture helps. This is Cisco's pointer processor again. This is a high level cartoon of it but it shows that the data is coming up in from the left. This is the multiplexed communications coming in from the left. This is the pointer processor. It has the three boxes that you saw before. The pointer interpreter that separates this data into the individual sections of RAM. They are represented by colors so each one of the STS's is represented by colors and interleaved and separated, the first STS, the second and the third into separate sections of RAM. That is an explanation of how one could describe it, and what it looks like. They're physically in different sections of RAM." Trial Tr. 1068-69 (Dr. Prucnal).

- "[T]his [PTX-388, illustrated in Prucnal demonstrative 35 reproduced below] is the description of what is inside of the pointer processor, and I said there is this thing called the RAM which is the memory. And this very explicitly shows in this case -- this is an STS-12 that this is dealing with in this particular document -- that the RAM, which is the memory, is divided into 12 sections, one for each STS-1. So there is a different section of memory, one for each

of the STS's and that indicates that the combined multiplex signal coming in is separated or demultiplexed to go into this RAM." Trial Tr. 1067 (Dr. Prucnal).



- "I referenced the pointer processor in regard to the demultiplexing that preceded the insertion of the error signal because there is demultiplexing there and that was important for the language of the claim." Trial Tr. 1120 (Dr. Prucnal).

- Trial Tr. 1151-1152 (Dr. Prucnal explaining why there is demultiplexing at the pointer processor).

As such, Cisco's blind contentions that "there is no dispute," "both experts agree," and "Dr. Prucnal conceded" (D.I. 376 at 4-5) the issue of whether the pointer processor is the demultiplexer directly conflict with the documents and testimony that Telcordia introduced at trial. Amazingly, Cisco bases its entire position that Telcordia conceded its case on the exact same out-of-context and cropped Prucnal deposition testimony that formed the basis for the same

argument that the Court rejected during the summary judgment phase of the case.[2] Specifically, during the cross-examination of Dr. Prucnal, Cisco's counsel merely read into the record the cropped and out-of-context passage from Dr. Prucnal's deposition testimony that was already considered and evaluated by the Court during summary judgment. Trial Tr. at 1126-28. Cisco's counsel's resurrection of a cropped passage from Dr. Prucnal's deposition testimony, however, did not persuade the factfinder and does not somehow negate the substantial evidence introduced by Telcordia at trial in support of its position that the pointer processor is the demultiplexer.

In addition to ignoring the substantial evidence and the Court's earlier summary judgment decision, Cisco further blurs the issue by ignoring a basic and non-controversial tenet of patent law: "[i]t is fundamental that one cannot avoid infringement merely by adding elements if each element recited in the claims is found in the accused device." *Stiftung v. Renishaw PLC*, 945 F.2d 1173, 1178 (Fed. Cir. 1991). Specifically, Cisco's brief focuses upon and reiterates the expert testimony, on both sides, recognizing that there is in fact an insertion of error signals before demultiplexing in Cisco's products ***in addition to*** insertion of error signals following the demultiplexing. D.I. 376 at 5, 10. But, as Cisco well knows, the fact that Cisco's products

[2] Specifically, during summary judgment Cisco argued that an isolated sound bite that its counsel obtained during Dr. Prucnal's deposition resulted in Telcordia conceding that only the cross connect, and not the pointer processor, could be the demultiplexer. D.I. 242, 269. In its answering brief, Telcordia explained in depth how Cisco had misconstrued the record, Dr. Prucnal's report, and Dr. Prucnal's testimony. D.I. 251. The Court agreed with Telcordia, finding no concession and instead finding that "there are genuine issues of material fact as to the 'inserting and error signal on designated ones of said [the] subrate communications' limitation, specifically whether the pointer processor in the defendants' accused products performs the recited function. More specifically, the court concludes that the dispute between the parties can be classified only as a classic battle of the experts." D.I. 341 at 13. Ignoring the Court's decision and ignoring the substantial evidence introduced at trial, Cisco resurrects the exact same passage from the Prucnal deposition to argue for the second time that "[b]ecause Dr. Prucnal conceded, as he must, that it is the cross-connect, not the pointer processor, that is the claimed demultiplexer, Cisco's non-infringement becomes purely a legal matter." D.I. 376 at 5. The issue is not a legal matter. Rather, as the Court has already ruled, it is a hotly disputed factual matter.

perform other operations ***in addition to*** the infringing operations does not save it from infringement. *Stiftung* 945 F.2d at 1178. Again, substantial evidence demonstrates that Cisco's products perform the following operations in the following order:

(1) **first insert line error signals** (AIS-L signals) at the receive framer (*see, e.g.*, Trial Tr. 1072 (Dr. Prucnal));

(2) **then demultiplex at the pointer processor component** (*see, e.g.*, Trial Tr. 1064-1066 (Dr. Prucnal describing demultiplexing at the "pointer interpreter" portion of the pointer processor));

(3) **then insert path error signals** (AIS-P signals) at the pointer processor component (*see, e.g.*, Trial Tr. 1065 (Dr. Prucnal describing insertion of AIS-P signals at the "pointer generator" portion of the pointer processor); and

(4) **then demultiplex at the cross-connect component** (*see, e.g.*, Trial Tr. 1065, 1069, 1123 (Dr. Prucnal describing the additional demultiplexing at the cross-connect component)).

See, e.g., Trial Tr. 1064-1073 (Dr. Prucnal); PTX-388; PTX-739. Substantial evidence, therefore, supports a finding that Cisco infringes because its products insert path error signals (AIS-P) in (3) above *following the demultiplexing* at the pointer processor in (2) above. That Cisco's products also insert different line error signals (AIS-L) before demultiplexing occurs (in (1) above), or that Cisco's products perform additional demultiplexing at the cross connect after the error signals are inserted (in (4) above), is entirely irrelevant to the infringement analysis. Cisco's focus on the operations performed by its products ***in addition to*** the infringing operations is a pedestrian effort at distraction, has nothing to do with whether substantial evidence supports the jury's verdict, and does not save it from infringement.

Indeed, knowing that performance of other operations *in addition to* the infringing operations does not save it from infringement, Cisco—in a last-ditch alternative argument—proceeds to try to alter the Court's already restrictive "following demultiplexing" limitation to require following the *ultimate* or the *final* demultiplexing. D.I. 376 at 6-7. Under Cisco's

theory, if the Court's construction dictated that the insertion of error signals must follow the *final* demultiplexing, then the other operations of Cisco's product (namely, the follow-on demultiplexing at the cross connect) could possibly save it from infringement. But Cisco offers no support or reason for its peculiar post-trial modification to the Court's straightforward claim construction. To re-construe the claims after trial would, obviously, turn the case on its head—Cisco did not advance its new, hyper-restrictive construction during the claim construction phase of the case. As such, Telcordia was never afforded an opportunity to respond to the merits, as a matter of claim construction, of Cisco's new post-trial construction. Moreover, both parties' infringement and validity theories throughout the summary judgment and trial phases of the case may have been far different under a different claim construction (*e.g.*, Telcordia could have explained to the jury that Cisco's products actually insert error signals again after what Cisco now conceives as the "final" demultiplexing). In short, there is no basis to modify, post-trial, the straightforward claim construction of "following demultiplexing" just to accommodate Cisco's legally incorrect theory that the collateral operations in its products save it from infringement.[3]

As a final alternative fallback argument, Cisco accepts that Dr. Prucnal did explain during trial that the pointer processor is a demultiplexer but contends that "there is simply no meaningful support in the record for Dr. Prucnal's opinion that the pointer processor performs the demultiplexing." D.I. 376 at 7. Obviously, Telcordia disagrees and again notes the above ample evidence of record showing the pointer processor performing demultiplexing. In advancing its position, however, Cisco argues that Dr. Prucnal defined "demultiplexing" during

[3] Indeed, the "following demultiplexing" limitation was advanced by Cisco, and disputed by Telcordia, during claim construction. Cisco should not now be permitted to suggest that "following demultiplexing" requires something more than it successfully advocated during the claim construction phase of the case.

trial to require that a signal is dropped, and that because the pointer processor does not drop a signal it cannot be a "demultiplexer." D.I. 376 at 8.

Cisco bases its argument on an outright mischaracterization of the trial record. Specifically, in its brief Cisco states that:

> Dr. Prucnal testified that a 'standard' definition for a demultiplexer in the context of the '763 patent is a device that receives a multiplexed signal as its input and drops at least one demultiplexed channel at its output. D.I. 354 at 1139:5-10.

D.I. 376 at 8. Cisco then concludes that "the pointer processor in Cisco's products does not satisfy even Dr. Prucnal's definition of demultiplexing." D.I. 376 at 7-8. But Dr. Prucnal never advanced the limited, restrictive, and incorrect definition of "demultiplexer" as a device that "drops at least one demultiplexed channel at its output" during trial. Indeed, the excerpt that Cisco cites from the trial transcript simply does not support Cisco's mischaracterization of Dr. Prucnal's definition:

> Q: And one of the ways of knowing whether you have got a demultiplexer is -- the standard definition of demultiplexer is where the input is a multiplexed stream, in other words, combined, and demultiplexed in the output, **it would be different streams, right, or something dropped?**
>
> A: Right.

Trial Tr. 1139:5-10 (Cross Examination of Dr. Prucnal). The question and answer, in fact, indicates—in the *disjunctive*—that a demultiplexer divides a combined signal into "different streams" ***or*** results in a signal that is "dropped." While a signal may be dropped at a demultiplexer, Dr. Prucnal's testimony most certainly does not, as Cisco now mischaracterizes, provide a standard definition for a "demultiplexer" that requires that a signal must be dropped. To the contrary, Dr. Prucnal always consistently maintained that a demultiplexer, quite simply,

takes a combined signal and separates it into constituent signals (irrespective of whether a signal is dropped):

- "That is separating from a single combined data stream into the separate portions the STS-1s. That is called demultiplexing." Trial Tr. 1066 (Dr. Prucnal).

- "The original high rate signal is broken down, in one example, from an OC 192, 192 STS-1s ones to four groups of 48. That is one demultiplexing." Trial Tr. 1150 (Dr. Prucnal).

Indeed, the Court recognized Dr. Prucnal's definition of demultiplexing in its summary judgment opinion:

> the parties' experts even dispute the meaning of "demultiplexing" - Telcordia's expert, Dr. Paul Prucnal ("Dr. Prucnal"), defines the term as **"[t]he separation from a common input into several outputs"** (D.I. 264 Ex. 3, at 4), while the defendants' expert, Dr. Wayne Grover ("Dr. Grover"), defines the terms as "separating the constituent channels out of a high-speed signal and restoring each channel to its original signal format." (D.I. 256 Ex. 3 ¶ 55.)

D.I. 341 at 13 (emphasis added). Dr. Prucnal maintained this same position at trial—he never abandoned his position as to "demultiplexing," and he never conceded that a demultiplexer must drop a signal as Cisco now mischaracterizes (indeed, neither expert ever advanced the restrictive, mischaracterized definition that Cisco now advances). Rather, in a desperate argument that "no reasonable jury could have found that the pointer processor performs demultiplexing," Cisco simply seizes upon an isolated portion of Dr. Prucnal's testimony, mischaracterizes the testimony, dismisses all context, ignores the remainder of the trial record, and issues its self-serving proclamation that "the pointer processor in Cisco's products does not satisfy even Dr. Prucnal's definition of demultiplexing." D.I. 376 at 7-8.[4]

[4] Cisco's brief is littered with over 30 proclamations in the nature of Telcordia "did not refute," "there is no dispute," "the testimony was undisputed," "both experts agree," Telcordia "conceded," Telcordia "had to agree," Telcordia "admitted," Telcordia "acknowledges," the (continued...)

But when Cisco's mischaracterizations of the record are repaired, it is clear that Telcordia presented ample evidence showing that the pointer processor in Cisco's products demultiplexes. Specifically, Dr. Prucnal, with reference to internal Cisco documents that describe the operation of Cisco's products, explained (1) that the pointer processor is a demultiplexer, (2) exactly how the pointer processor demultiplexes the signal, and (3) exactly when and why, in the context of the environment of the product as a whole, the pointer processor demultiplexes the signal. As such, the jury's verdict of infringement is clearly supported by substantial evidence.

2. Substantial Evidence Demonstrates that the Pointer Processor Inserts Error Signals Following Demultiplexing in Response to a High-Level Failure

In its motion, Cisco attempts to equate the line error signals (AIS-L) with the path error signals (AIS-P) in an effort to argue that there can be no infringement because the AIS-L line error signals—the only error signals according to Cisco—are inserted before, not following, the demultiplexing. D.I. 376 at 11. Specifically, Cisco ignores the distinction between the two different error signals and argues that "once the framer inserts an all ones error signal [AIS-L] in response to a high-level failure, those same ones 'are simply propagat[ed] down through all the subsequent block elements and components of the system.'" *Id.* In essence, under Cisco's theory, it is as if the AIS-P path error signals—those which form the basis of Telcordia's infringement contentions—never existed. The logical breakdown in Cisco's theory (i.e., that two

---

(…continued)
"facts are undisputed," "Telcordia presented no evidence," etc. D.I. 376. While Telcordia appreciates the benefit of presenting neutral, truly undisputed facts and issues to the Court in an effort to streamline and narrow matters, Cisco's proclamations in its JMOL brief are liberal mischaracterizations on hotly contested issues. While some of Cisco's mischaracterizations are more flagrant than others, Telcordia cannot possibly (within the limits of its brief) address each instance. Suffice it to say, Telcordia disputes all of Cisco's liberal mischaracterizations that Telcordia admits, concedes, does not dispute, offers no evidence, etc., as to the key issues in this case. The trial record speaks for itself and simply does not support Cisco's mischaracterizations.

different signals, with different names, inserted at different points in the products, for different reasons, are nevertheless the same—and hence one of the signals should just be forgotten), however, was squarely presented to the jury. The jury was free to decide whether the AIS-L signal is the only error signal (and that Cisco does not infringe because that only signal is inserted before, not following, demultiplexing), or alternatively whether the separately named, separately diagramed AIS-P signal in fact exists and in fact is inserted following the demultiplexing to yield infringement. The jury's decision, as demonstrated below, is supported by substantial evidence.

Cisco alternatively argues that only the AIS-L signals, and not the AIS-P signals, can be inserted "in response to a high level failure" as required by the claims. D.I. 376 at 10-12. Again, the relevant technical documentation and the experts' competing views on the issue were squarely before the jury. Again, as demonstrated below, substantial evidence supports the jury's determination.

To revisit the operation of Cisco's products as established at trial, substantial evidence shows that Cisco's products perform the following operations in the following order:

(1) **first insert line error signals** (AIS-L signals) at the receive framer (*see, e.g.*, Trial Tr. 1072 (Dr. Prucnal));

(2) **then demultiplex at the pointer processor component** (*see, e.g.*, Trial Tr. 1064-1066 (Dr. Prucnal describing demultiplexing at the "pointer interpreter" portion of the pointer processor));

(3) **then insert path error signals** (AIS-P signals) at the pointer processor component (*see, e.g.*, Trial Tr. 1065 (Dr. Prucnal describing insertion of AIS-P signals at the "pointer generator" portion of the pointer processor); and

(4) **then demultiplex at the cross-connect component** (*see, e.g.*, Trial Tr. 1065, 1069, 1123 (Dr. Prucnal describing the additional demultiplexing at the cross-connect component)).

During trial, Telcordia's expert explained exactly how and why there is a difference between AIS-L error signals (the line error signals noted at (1) above—before demultiplexing) and AIS-P error signals (the path error signals noted at (3) above—following demultiplexing):

> Q. Okay. And let's talk about the error signal for a minute. Still using your Slide No. 11, this is a chip here called the receive framer chip. Do you see that?
>
> A. Yes.
>
> Q. I will label that one No. 4. That chip also inserts error signals, doesn't it?
>
> A. It inserts another type of error signal. The claim requires that the error signals are ones that are inserted on the individual STS1s. On the individual subrate channels, the error signals inserted on 4 are the line-level signals, which is not at the individual level. They are different than the error signals inserted on 3, which are the AIS-P's.
>
> Q. So let's make sure we have the terminology right. There is two types of error signals. One is called line signals, and that's AIS-L, and one is path signals, which is AIS-P. Correct?
>
> A. Those are two different types, yes.

Trial Tr. 1130-31, *see also* Trial Tr. 1135-36 (Dr. Prucnal). As such, substantial evidence supports the jury's determination that the AIS-L signals are not the same as the AIS-P signals, and that the AIS-P signals cannot simply be ignored in the infringement analysis.

In the alternative, Cisco acknowledges that the AIS-P signals exist, but argues that no reasonable jury could have found that the AIS-P signals are inserted in response to a high-level failure as required by the claims. D.I. 376 at 10-12. Specifically, in its brief Cisco notes that only the error signals inserted at the framer (*i.e.*, the AIS-L signals in (1) above) are inserted in response to a high-level failure. D.I. 376 at 10. But again, Cisco simply ignores the substantial evidence that Telcordia introduced establishing that the error signals inserted at the pointer processor (*i.e.*, the AIS-P signals in (3) above) are inserted in response to a high-level failure.

Specifically, Telcordia's expert explained exactly how and why the AIS-P signals are inserted in response to a high-level failure on numerous occasions:

- "Remember, I said that there was a monitoring means that was looking to see if the signal was absent or if there was some problem at the high level of the multiplex signal? That monitoring means generated the loss of signal or the loss of frame. And then in response to, this pointer processor, this is in the pointer generator, after demultiplexing, has generated the error signal on the individual STS-1s." Trial Tr. 1067-68 (Dr. Prucnal).

- "Q: So if that framer -- and the claim is talking about inserting an error signal in response to detecting a high-level fault. Right?

  A: Yes. If I can explain what happens, you just pointed out that at the receive framer chip, No. 4, if there is a loss of signal or loss of frame, all of those 1's are generated and they go down into the next portion of the chip. As I said, in addition to that, coming out of the receive framer is another signal that goes directly to the pointer processor to tell it to insert the new 1's, the AIS-P." Trial Tr. 1133 (Dr. Prucnal)

- "Q: Exactly. The receive framer. That receive framer is detecting a line-level fault, a high-level fault. Right?

  A: Yes.

  Q: And in response to that detection of a high-level fault, the receive framers puts 1's everywhere?

  A: In addition to generating a signal that comes down to here, yes.

  Q: When you say here, you are referring to No. 5, the pointer generator?

  A: It is that little arrow down at the bottom.

  Q: Right there. Right?

  A: Yes.

  Q: And in response to that signal from the receive framer, the pointer generator adds these 1's into the bit stream. Correct?

  A: It is actually creating a new bit stream at that point.

  Q: It is adding the 1's, as you described?

  A: Yes.

> Q: The pointer generator is generating those 1's in response to the signal from the receive framer. Right?
>
> A: Right.
>
> Q: And the receive framer is the one that had detected the line fault originally, wasn't it?
>
> A: Yes. For the description of what happens when there is a line fault, that's what occurs. I could point out that the AIS-L signal in the pointer interpreter also generates another AIS-P alarm, in addition to what I have described." Trial Tr. 1137-38 (Dr. Prucnal).

In summary, Dr. Prucnal explained that (1) the receive framer detects a high-level failure, (2) the receive framer then inserts AIS-L signals and sends another signal directly to the pointer processor, and (3) in response, the pointer processor inserts AIS-P signals. As such, substantial evidence supports the jury's determination the AIS-P error signals are inserted in response to a high-level failure as required by the claims.

B. Substantial Evidence Supports the Jury's Finding that the Means-Plus-Function Claims of the '763 Patent Are Not Invalid as Indefinite

The jury expressly found that asserted claims 1, 2, 7, and 8 of Telcordia's '763 patent are not invalid. D.I. 348 at 4. In challenging the jury's verdict, Cisco now contends that no reasonable juror could have found that the '763 patent is not invalid because, according to Cisco, the '763 patent does not identify structure corresponding to the function of the "monitoring means" and is thus indefinite under 35 U.S.C. § 112, ¶2. D.I. 376 at 12-16. This is now the fourth time Cisco raises the exact same argument—having been rejected three times before, first during claim construction, then during summary judgment, and again during the jury trial. Substantial evidence clearly supports the jury's conclusion that asserted claims 1, 2, 7, and 8 of the '763 patent are not invalid as indefinite.

At the outset, the decision on definiteness is well within the province of the jury under Federal Circuit law. *BJ Servs. Co. v. Halliburton Energy Servs., Inc.*, 338 F.3d 1368, 1372 (Fed.

Cir. 2003)("[D]efiniteness . . . is amenable to resolution by the jury where the issues are factual in nature."). Indeed, during the summary judgment phase of the case, and in accordance with the Federal Circuit's *Halliburton* case, the Court ruled that "it seems to me that this [definiteness of the '763 patent] is a matter that should be resolved by the jury. I think there are material factual disputes." Sept. 18, 2006, Tele-hearing Tr. at 42. Those material factual disputes have now been resolved by the jury's verdict, which is based on substantial evidence.

In its Claim Construction Order, the Court determined that the "monitoring means" limitation in the asserted claims is a means-plus-function limitation pursuant to 35 U.S.C. § 112, ¶6. D.I. 179 at ¶8. The Court found that the function of the monitoring means is "evaluating the integrity of the multiplexed subrate communications on the first ring and the second ring," whereas the corresponding structure is "the circuitry at a controller that determines if a defect exists with the multiplexed subrate communications, and all equivalents thereof." *Id.* Cisco now attacks this limitation for the fourth time, once again contending (1) that there is no disclosure of corresponding structure in the specification, and, alternatively, (2) that there is no linking of structure in the specification to the function of the monitoring means. But substantial evidence demonstrates that the '763 patent specification clearly discloses and links structure—the controller—corresponding to the function of the "monitoring means" as construed by the Court.

Specifically, as Dr. Prucnal testified on cross-examination during trial:

> Q: Now, when you looked in the patent, you didn't actually find any structure, did you, for performing this monitor means function? Any actual structure, circuitry?
>
> A: Well, there was no circuit diagram but **the controller was described** and what it had to do was described and for someone of ordinary skill in the art, they would know how to interpret this and actually build a circuit.

Trial Tr. 1147 (Dr. Prucnal). Dr. Prucnal also explained why disclosure of circuit details would be impractical:

> . . . in a patent like this that is describing the whole network and the protection path, the protection switching that would occur, one could not describe all the details at every circuit. So I just conclude from what they describe, someone would know, of ordinary skill would know how to do it.

Trial Tr. 1147-48 (Dr. Prucnal). Dr. Prucnal's testimony is consistent with the controlling Federal Circuit law on the disclosure of structure, which does not require that the specification disclose the details of the circuitry in order to meet the definiteness requirement. *Intel Corp. v. Via Techs., Inc.*, 319 F.3d 1357, 1365-66 (Fed. Cir. 2003)(rejecting infringer's contention that "generic core logic is an inadequate disclosure of structure because no circuitry is disclosed in the patent . . ." where the court's construction dictated that the corresponding structure to perform the claimed function was "the core logic of a computer modified to perform Fast Write.")

Moreover, Dr. Prucnal expressly identified the controllers 117 and 118 as structure associated with the function of the "monitoring means":

> Q: Looking at Figure 1, which circuits are the monitoring means that you were talking about in this figure?
>
> A: The controller.
>
> Q: And just for the record, identify the controllers, please?
>
> A: There is a controller 118. The switch is represented by this box. And 117, that is represented by this box. And then each of the nodes has the two controllers, like that.
>
> . . .
>
> Q: So where are the circuits that you were referring that is part of the monitoring means?
>
> A: Yes. As I said, the circuits are in the controller.

Trial Tr. 1149. Importantly, Dr. Prucnal did not, as Cisco suggests, testify that there is no structure disclosed in the specification. Nor did Dr. Prucnal testify that one skilled in the art would only inherently know what structure would be needed to perform the function of the "monitoring means." To the contrary, Dr. Prucnal testified that structure is disclosed in the specification and that a person of skill in the art would know—from the structural disclosure of the controllers found in the specification—how to implement the "details at [the] circuit." Dr. Prucnal's testimony that a person of skill in the art would understand the controllers 117 and 118 to be the structure corresponding to the monitoring means is consistent with Federal Circuit law, which explains that the inquiry is "whether one of skill in the art would understand the specification itself to disclose a structure, not simply whether that person would be capable of implementing a structure." *Biomedino, LLC, v. Waters Tech. Corp.*, No. 2006-1350, slip. op. at 11 (Fed. Cir. June 18, 2007). Again, the issue is not one of enablement as Cisco suggests—Dr. Prucnal did not testify that a person of skill in the art would be capable of implementing a structure despite the lack of structural disclosure in the specification. Rather, Dr. Prucnal explained that to a person of skill in the art, the '763 patent specification in fact discloses the structural elements necessary to perform the function of the monitoring means.[5]

---

[5] Cisco's motion blurs the clear distinction between (1) relying upon the knowledge of one skilled in the art to inherently understand structure where no structure is disclosed in the specification—which would be improper, and (2) relying upon the knowledge of one skilled in the art to understand the structure that is disclosed in the specification—which is proper. The evidence that Telcordia presented at trial supports the latter, proper analysis, not the former, improper analysis. There is nothing improper, as Cisco suggests, in Telcordia's reliance upon how a person of skill in the art would understand the structural disclosure in the specification. Indeed, the Federal Circuit instructs that:

> Whether the specification adequately sets forth structure corresponding to the claimed functions must be considered from the perspective of one skilled in the art. *Budde v. Harley-Davidson, Inc.*, 250 F.3d 1369, 1376 (Fed. Cir. 2001). Any fact

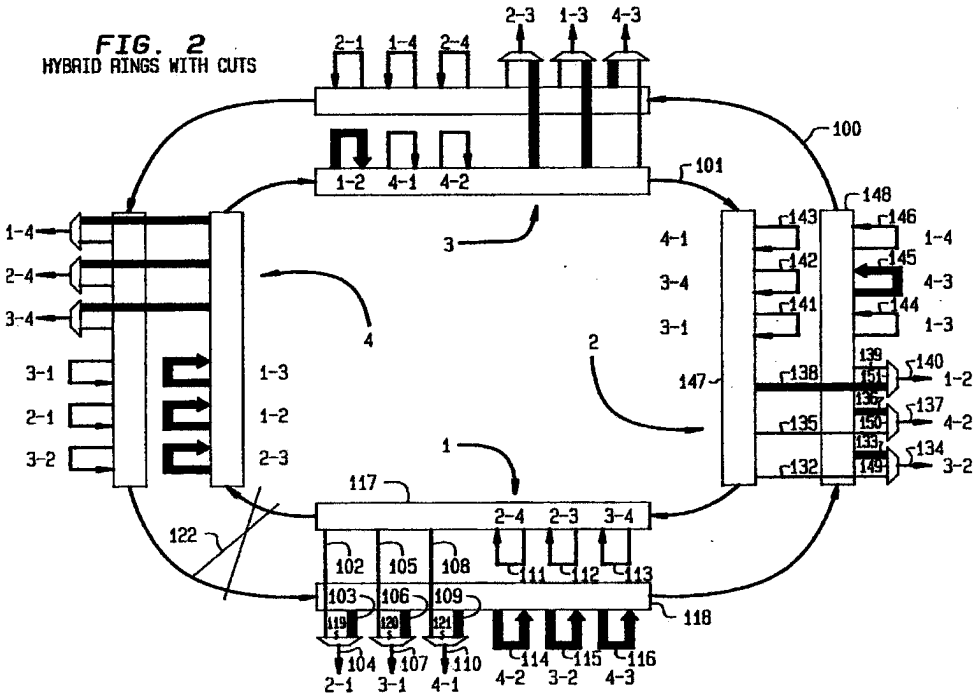
(continued...)

Dr. Prucnal's testimony is entirely consistent with the Court's construction and the '763 patent specification—both of which were before the jury. For instance in the '763 patent, the structure that Dr. Prucnal identified—controllers 117 and 118—are disclosed and discussed in detail (not merely in "black box" form). For example, Fig. 2 discloses controllers 117 and 118, including the illustration of, *inter alia*, exactly where in the structure of the larger ring network the controllers are found, how the structure of the controllers is integrated into the network (i.e., one on each of the two counter-rotating rings), how the structure of the controllers interrelates with other structural components in the network, and how the respective signals move through the structure of the controllers:

(...continued)

> critical to a holding on indefiniteness, moreover, must be proven by the challenger by clear and convincing evidence. *See id.* at 1376-77. In this case, [a challenger] needed to prove, by clear and convincing evidence, that the specification lacks adequate disclosure of structure to be understood by one skilled in the art as able to perform the recited functions.

Intel Corp. v. Via Techs., Inc., 319 F.3d 1357, 1365-66 (Fed. Cir. 2003).



Similarly, the specification discloses the structure and operation of the controllers in detail—particularly with reference to the function of the monitoring means:

> Each node continuously **monitors and evaluates the integrity of the multiplexed subrate signals** arriving at the node. Illustratively, this could be accomplished by detecting the absence of a carrier signal in an analog signal environment, or the lack of any incoming signal in a digital environment. When node 1 recognizes major line fault 122 in ring 100, **controller 118** inserts an error signal onto the six subrate channels. This could illustratively be accomplished by inserting a string of 1's on each channel in a digital environment.

PTX-7 col. 3, ll. 4-13. In this passage of the specification, the structural element (controller 118) is expressly linked to the function of the monitoring means as construed by the Court (evaluating the integrity of the multiplexed subrate signals).

Cisco simply failed to establish, by clear and convincing evidence, that the '763 specification lacks adequate disclosure of structure to be understood by one skilled in the art as able to perform the function of the monitoring means. The jury was properly instructed to determine "whether the '763 patent describes a structure for the monitoring means and whether it

links that structure to the function of the monitoring means," (Trial Tr. 2125) and that in doing so "[i]t is not proper to look to the knowledge of one skilled in the art apart from and unconnected to the disclosure of the patent." *Id.* Having been properly instructed, the jury decided that the '763 patent disclosed adequate structure to perform the function of the monitoring means. The jury's determination is clearly based upon substantial evidence—including Dr. Prucnal's testimony and the '763 patent.

IV. The '633 Patent

A. Substantial Evidence Supports the Jury's Determination that the '633 Patent Is Not Invalid for Obviousness

Cisco contends that no reasonable jury could have determined that the '633 patent is not invalid in light of the Gonzales reference (which was before the USPTO during examination). D.I. 376 at 19-28. To the contrary, substantial evidence supports the jury's determination that the '633 patent is not invalid in light of Gonzales, and that Cisco failed to establish by clear and convincing evidence that the '633 patent is invalid.

At the outset, Cisco's own expert testified at trial that "[i]t's my opinion that as construed by the Court, applying the claims as construed by the Court, Gonzales does not disclose all of the elements of the asserted claims." Trial Tr. 1691-92 (Dr. Acampora). Recognizing that the Gonzales reference alone fails to invalidate, Dr. Acampora had to resort to a theory that one of skill in the art would apparently supply the missing elements from the asserted claims with general knowledge. Cisco's position that the SRTS invention is nothing more than "common sense" was a stretch at best—the evidence at trial established invention of the '633 patent was specialized, elegant, complex, and highly regarded by persons of skill in the art—and the jury rightly rejected Cisco's position. Cisco's position now—that no reasonable juror could have rejected Cisco's aggressive obviousness theory—is an even greater stretch.

Specifically, although Cisco contended that the general knowledge of a person of skill in the art would supply the missing limitations from the Gonzales reference, Cisco did not actually present testimony establishing—on a claim element by claim element basis—all of the missing limitations that needed to be supplied from general knowledge (or more importantly how and why a person of skill in the art would supply those limitations). For example, during trial Telcordia established that the modulo 16 counter (a limitation of asserted claims 11 and 33) was not found in the Gonzales reference (and hence would need to be supplied by general knowledge under Cisco's obviousness theory):

> Q. In providing your testimony on direct examination, I don't want an opinion now, in providing your opinion testimony on direct examination, you never made any statement regarding whether Gonzales had a modular 16 counter. Is that true?
>
> A. In my testimony today?
>
> Q. Yes.
>
> A. I believe that's true.

Trial Tr. at 1693 (Dr. Acampora). But Dr. Acampora failed to offer any testimony suggesting that a modulo 16 counter would be something that a person of skill in the art would just generally know and combine with the Gonzales reference.

Additionally, the specialized, novel *residual* time stamp of the '633 patent consists of "the modulo 16 count of derived network clock cycles in the RTS period." PTX-1 col. 11, ll. 55-59; col. 16, ll. 17-22. But Dr. Acampora failed to offer any testimony suggesting (1) that Gonzales counts derived network clock cycles modulo 16 in an RTS period, or (2) that Gonzales transmits an RTS that is equal to the modulo 16 count of derived network clock cycles in an RTS period, which are elements (c) and (d) of claims 11 and 33. *Id.* Indeed, Gonzales does not disclose these elements and just as in the case of the modulo 16 counter, Dr. Acampora never

testified that elements (c) and (d) of claims 11 and 33 would be within the general knowledge of a person of skill in the art and would be combined with the Gonzales reference. Indeed, in providing his obviousness opinion, Dr. Acampora simply failed to analyze the language of the '633 patent claims in any respect whatsoever. As such, the evidence is consistent with Telcordia's position—the time stamp disclosed in the Gonzales reference (what Cisco calls the shortened time stamp of Gonzales) is not the specialized, novel *residual* time stamp of the '633 invention.[6]

Instead of addressing the exact claim limitations that are missing from Gonzales, at trial Dr. Acampora offered only the same conclusory allegations that Cisco offers in its JMOL motion—that a person of skill in the art would "through common sense" arrive at the SRTS invention from the Gonzales reference. D.I. 376 at 26. In performing its "common sense" analysis, Cisco first reduces the SRTS invention—ignoring the express language of the asserted claims—to two important, but grossly oversimplified, characteristics: (1) "the transmission of a shortened time stamp," (2) "outside of the convergence sublayer overhead." D.I. 376 at 21. Having reduced the entirety of the asserted '633 claims to these two characteristics for purposes of its obviousness analysis, Cisco then argues that a person of skill in the art would easily "put two and two together" (i.e., Gonzales' supposed disclosure of a shortened time stamp and a

[6] Indeed, Cisco wrongly contends that Gonzales teaches a shortened time stamp. Specifically, Cisco contends that Mr. Houdoin's testimony "establishes that a person of ordinary skill in the art would read the disclosure of Gonzales to teach a shortened time stamp." D.I. 376 at 23. But Mr. Houdoin's testimony does not support this conclusion. Mr. Houdoin only testified that "in Page 9.4.5 it says that only two bits are needed to represent the value of delta X." Trial Tr. 1488. But the disclosure on page 9.4.5 of Gonzales, in fact, reiterates that there is a "2-bytes field reserved for sending clock information" and that even though "only 2 bits are needed to represent the value of dX . . . the remaining bits can be used to protect the information from errors." DTX 2046. In other words, Gonzales discloses a time stamp that remains at 2-bytes in size (but that sends redundant information to protect from errors). In short, neither the Gonzales disclosure nor the Houdoin testimony supports Cisco's position that Gonzales discloses a shortened time stamp.

skilled artisan's apparent instinct to move that shortened time stamp outside of the convergence sublayer). D.I. 376 at 22.

The jury rightly rejected Cisco's shortcut approach. But even if Cisco's shortcut approach (*i.e.*, focusing on a simplified abstraction of the invention for obviousness purposes rather than on the language of the claims) were appropriate, Cisco's expert never explained how or why a person of skill in the art would know to move the time stamp of Gonzales from the convergence sublayer to outside of the convergence sublayer. Indeed, Dr. Acampora offered only extraordinarily conclusory testimony on this point:

> Back up just one moment. Another aspect of the obviousness is, it's not drawn directly from this article [Gonzales], but one of skill in the art would recognize, **for reasons that I mentioned earlier**, if you can take the information out of the rigid confines of a layer in a protocol stack, do it. That would be obvious to anyone.

Trial Tr. at 1560 (Dr. Acampora). This conclusory statement unsurprisingly proved to be entirely inadequate in convincing the jury that the invention was obvious. Moreover, the only "reasons mentioned earlier" by Dr. Acampora actually weigh against finding that it would be obvious to one of skill in the art to shuffle the Gonzales time stamp from one layer to another:

> In telecommunications, we have very rigidly defined communication protocols. The protocols are generally represented by seven functions. We speak of a seven-layer protocol stack. The responsibilities of each layer are rigidly defined by standards. They are rigidly defined because each layer is dependent upon the contribution of each other layer. So if I have a layer up here and a layer down here isn't doing the job, the layer up here won't work. Going back to the mail analogy. When I send a letter to one of you, I write the letter, put it in an envelope, I write the address on it, I drop it in the post box, I am assuming somebody is going to come by and pick that letter up. I am assuming that person is going to have a truck. Somebody put gas in the truck. Somebody made sure the tires weren't flat. The truck is going to come by and pick up that letter. If the truck doesn't pick of the letter, if it ran out of gas or got a flat tire, my letter doesn't get sent.
>
> Protocols are not that different. The higher layers are dependent upon some service provided by the lower layer. So when you put something

> into a layer in a communication protocol, it is rigid. It is there. You got to do it. No two ways about it. It has become your responsibility. The buck stops here.
>
> So if I assign the responsibility of delivering timing information to circuit emulation to a particular layer, that layer is stuck with it. The buck stops there. It's got to be done.

Trial Tr. 1549-50 (Dr. Acampora). Thus, even if Cisco's shortcut obviousness analysis were appropriate, Dr. Acampora's testimony about the layers in a telecommunications protocol stack certainly does not support his later conclusory opinion that "if you can take the information out of the rigid confines of a layer in a protocol stack, do it. That would be obvious to anyone." To the contrary, Dr. Acampora's explanation of the layers in a protocol stack clearly suggests that one of skill in the art most certainly would not simply shuffle timing information out of its designated layer and place it in a different layer (*e.g.*, "if I assign the responsibility of delivering timing information to circuit emulation to a particular layer, that layer is stuck with it. The buck stops there. It's got to be done.").

In sum, Cisco's position that the novel aspects of synchronous residual time stamp technology are simply a matter of "common sense" (D.I. 376 at 26) is a result of a flawed, oversimplified analysis and stands unsupported in the record. Moreover, even if the jury were inclined to accept Cisco's oversimplified approach—which it obviously was not—Cisco's evidence did not support its theory that one skilled in the art would have just moved the time stamp from inside to outside of the convergence sublayer. To the contrary, the testimony presented by Cisco's expert suggests just the opposite—that one skilled in the art would understand not to move anything that had been assigned to a specific layer in a protocol stack. As such, the jury's rejection of Cisco's strained obviousness theory is entirely reasonable on numerous grounds.

Finally, although the '633 patent enjoys a presumption of validity, and although it was not Telcordia's burden to establish non-obviousness, the jury was nevertheless presented with ample evidence establishing non-obviousness of the '633 patent. Most notably, the secondary considerations presented to the jury weighed heavily in favor of a finding of non-obviousness.[7] For example:

- As to commercial success and industry acceptance, the evidence at trial established that many companies recognized the value and importance of SRTS. PTX-5000 (Ex. A); Trial Tr. 286-87, 360-61 (Mr. Giordano). Indeed, the evidence established that the technology was expressly adopted by the International Telecommunications Union, the American National Standards Institute, and the ATM Forum. Trial Tr. 1180-87 (Dr. Walters). The evidence also showed that Cisco's products were expressly marketed as SRTS-capable, and that the products enjoyed significant sales in the market. Trial Tr. 1161-63 (Mr. Fedorkow); 1414-16 (Mr. Carroll); 1308-09 (Mr. Nawrocki); PTX 355; PTX 356; PTX 1242; PTX 1370; PTX 1375; PTX 1376, PTX 1404. The evidence at trial also established that over 15 companies in the telecommunications industry, including well-known companies such as NEC, Fujitsu, Siemens, and Newbridge, licensed Telcordia's SRTS technology.[8] PTX-5000 (Ex. A); Trial Tr. 286-87, 360-61 (Mr. Giordano); DTX 2569. These licenses are "strong indicia" of non-obviousness under Federal Circuit law. *WMS Gaming Inc. v. International Game Technology*, 184 F.3d 1339, 1360 (Fed. Cir. 1999).

- As to professional recognition, the evidence at trial established that Cisco's own patent states that "the synchronous residual time stamp clock recovery method" is "commonly used" (Trial Tr. 1698; PTX-1417), another patent indicates that SRTS is "perhaps the most elegant and widely accepted clock recovery scheme," (Trial Tr. at 1699), and that SRTS was the subject of a publication in a prestigious peer-reviewed journal (Trial Tr. 1700).

- As to unexpected results, the evidence established that Dr. Lau was initially "somewhat incredulous" about the initial ideas behind SRTS because "it represented a large improvement." Trial Tr. 578.

---

[7] The fact that Dr. Acampora testified that relevant secondary considerations weighed in favor of finding obviousness (D.I. 376 at 27-8) misses the point. The issue here is whether there is substantial evidence supporting Telcordia's position.

[8] A number of additional license agreements—including the Lucent / Alcatel license that resulted from a settlement just before trial and the FORE Systems license that resulted from the settlement of an earlier litigation—were not before the jury.

- As to copying, the evidence at trial established that Cisco directly copied Telcordia's patented SRTS technology by (1) purposefully building its products to comply with established SRTS standards, and (2) incorporating a chip into its products where the specification for the chip expressly warned that the chip "contains SRTS logic that Bellcore holds the patent on." Trial Tr. 819-20; PTX 1366; *See* Telcordia's Brief in Support of Its Motion to Enhance Damages, D.I. 370 at 4-7 (detailing ample evidence establishing that Cisco copied Telcordia's SRTS technology).

The jury's decision that the '633 patent is not obvious in light of the Gonzales reference is thus clearly supported by substantial evidence.

B. Substantial Evidence Supports the Jury's Determination that the '633 Patent Is Not Invalid for Improper Inventorship

During trial and in its JMOL motion, Cisco argued that the '633 patent is invalid because individuals at France Telecom allegedly contributed to the patent but were not named as inventors on the patent. D.I. 376 at 28-32. The jury rejected Cisco's theory. Substantial evidence supports the jury's determination that Cisco failed to establish invalidity due to improper inventorship by clear and convincing evidence.

At the outset—perhaps the most telling flaw in Cisco's improper inventorship theory—no one at France Telecom has ever claimed to be an inventor of the SRTS patent.[9] In other words, Cisco's theory is entirely self-serving and litigation driven—it is not even supported or advanced by the very individuals that Cisco claims are the supposed joint inventors. Indeed, despite deposing all three of the key France Telecom employees (Pierre Adam, Thierry Houdoin, and Jean-Yves Cochenec), despite its codefendant's suggestive statement to France Telecom before the depositions—"[i]t will be very helpful to Alcatel, and it could turn out to be in France Telecom's interest, to discover the extent to which its own engineers may have contributed to an

[9] Indeed, nobody at France Telecom raised any kind of issue or concern whatsoever over Telcordia's SRTS patent until the depositions of the France Telecom witnesses in this case in April of 2006—a full 15 years after the 1991 communications between France Telecom and Bellcore.

invention that Telcordia has long claimed as its own and for which Telcordia's engineers have taken all the credit," (Trial Tr. 1508)—and despite Cisco's private meetings with each of the supposed France Telecom inventors before their depositions (Trial Tr. at 1504-06), no one from France Telecom ever testified that he was an inventor or co-inventor of SRTS.

Undeterred by its failure to establish an inventorship problem during discovery, Cisco nevertheless cobbled together and presented an improper inventorship theory to the jury through a series of sketchy facsimile communications between Bellcore and France Telecom (the six facsimile exchanges include DTX 2367 through 2372). But, consistent with the fact that none of the France Telecom employees actually claimed to be an inventor when they were deposed on the matter, the documents presented by Cisco simply do not establish, by clear and convincing evidence or otherwise, that the '633 patent is invalid for improper inventorship.

The primary France Telecom document on which Cisco relies to support is improper inventorship theory is an August 26, 1991, fax from Pierre Adam to Bellcore. PTX 518, DTX 2367; D.I. 376 at 30-32. Specifically, Cisco contends that the August 26, 1991, fax reflects France Telecom's contribution of the idea of "a shortened time stamp" and "transmission of that time stamp outside the convergence sublayer overhead" to the inventors Dr. Lau and Dr. Fleischer. D.I. 376 at 30-32. But evidence introduced at trial establishes that the fax does not disclose any aspect, let alone the key aspects, of the SRTS invention. For example, the August 26, 1991, fax, which consists of five sentences on half of a page of paper, does not disclose counting derived network clock cycles modulo 16 in an RTS period or transmitting an RTS (in overhead other than the convergence sublayer overhead) that is equal to the modulo 16 count of derived network clock cycles in an RTS period. Trial Tr. 660-61, 1475-6 (Mr. Adam), 1489, 1689 (Dr. Acampora).

Moreover, the fax contains no contribution toward the SRTS invention because substantial evidence shows that it is directed to the traditional 2 byte (16 bit) time stamp not to any type of shortened time stamp and certainly not to the specific *residual* time stamp of the SRTS invention. *See, e.g.*, Trial Tr. 599-600 (Dr. Fleischer), 689, 794-95 (Dr. Lau), 1448, 1451-52 (Mr. Adam), 1689 (Dr. Acampora). In fact, consistent with Telcordia's position that the SRTS *residual* time stamp was Bellcore's idea, the very first mention of a *residual* time stamp (at first called a "residue" time stamp) appears not in the fax from France Telecom to Bellcore but rather in a later fax from Bellcore to France Telecom—"[u]se of the residue-TS to convey the frequency difference between the service and the network clock." DTX 2369 (October 11, 1991, fax from Bellcore to France Telecom). Again, in contrast, the August 26, 1991, fax from France Telecom to Bellcore upon which Cisco relies for improper inventorship only discusses the traditional time stamp. DTX 2367. In fact, France Telecom's first recognition of Bellcore's *residual* time stamp was not in its August 26, 1991, fax, but rather in a later fax in response to Bellcore's October 11, 1991, fax that first disclosed the *residual* time stamp (again, then called a "residue" time stamp). Specifically, in response to Bellcore's October 11, 1991, disclosure of the "residue" time stamp, France Telecom capitulated that "we agree with your observation: the TS conveys redundant information and in fact 2 bits are sufficient for a correct operation." PTX-521 (October 14, 1991, fax from France Telecom to Bellcore).

Given that the August 26, 1991, France Telecom fax only disclosed the traditional time stamp, not a shortened time stamp and not the *residual* time stamp of the SRTS invention, Cisco argued alternatively to the jury that the fax nevertheless contained an inventive contribution because it suggested moving the traditional time stamp from the convergence sublayer into the SAR layer:

> And here is the proposal. You take the time stamp from the French method, you take the SAR header from the SFET method, you combine them together, and that's SRTS.

Trial Tr. at 2208 (Cisco closing argument). Cisco's simplistic analysis of the France Telecom fax, however, suffers from numerous flaws (as the jury correctly determined). First of all, the invention of SRTS does not involve taking the "time stamp from the French method" (i.e., a traditional 16 bit time stamp) and placing it in the SAR header. That is not SRTS. Again, as demonstrated by substantial evidence at trial, SRTS involves (and the claims of the '633 patent expressly require) a specialized, novel *residual* time stamp that consists of "the modulo 16 count of derived network clock cycles in the RTS period." PTX-1 col. 11, ll. 55-59; col. 16, ll. 17-22. As such, France Telecom's proposal to simply move the traditional time stamp to the SAR layer has nothing to do with the invention of SRTS—which involves a specific *residual* time stamp.

Moreover, as Cisco recognized in its closing argument (Trial Tr. 2208 noted above), and as the documents and testimony introduced at trial clearly establish, the use of the SAR layer to transmit timing information was not a novel suggestion but rather had long been part of Bellcore's prior SFET technique for timing recovery. PTX-519, Trial Tr. 590 (Dr. Fleischer), Trial Tr. 689-90 (Dr. Lau). In other words, France Telecom's recognition in its August 26, 1991, fax of the possibility of transmitting timing information in the SAR layer is nothing more than a recognition of a prior principle found in Bellcore's earlier SFET technique—it most certainly is not an inventive contribution to SRTS. Trial Tr. 609 (Dr. Fleischer), Trial Tr. 689-90 (Dr. Lau). Even the France Telecom witnesses acknowledged during trial that their proposal to move the time stamp from one layer to another was simply done in conformance with the "Bellcore scheme":

> So we were leaving one layer to another, to the **Bellcore layer**. We were leaving our parallel way to proceed to a serial way, to proceed **according**

> **to the Bellcore scheme**, and this was the proposal we forwarded to the Bellcore team…
>
> . . .
>
> So the, the spirit of our way to look for a compromise was to, to take our way to proceed and to transfer this information **according to the Bellcore scheme in the SAR** on the reserved bit on the second cell basis.

Trial Tr. 1448, 1452 (Pierre Adam).

Moreover, a prior June 6, 1991, internal Bellcore engineering memorandum establishes that Bellcore not only earlier had the idea of transmitting timing information in the SAR layer (as established above), but also that Bellcore earlier had the idea of transmitting a shortened time stamp in the SAR layer. PTX-519.[10] Specifically, Dr. Lau testified that the June 6, 1991, memo discloses carrying timing information in the SAR layer in as little as one bit. Trial Tr. 682-83, *see also* Trial Tr. 654 (Dr. Fleischer describing the one bit counter).

In sum, substantial evidence supports the jury's conclusion that the August 26, 1991, fax from France Telecom to Bellcore did not contain any contribution toward Bellcore's SRTS invention. Additionally, while the '633 patent is presumed valid, and while it was not Telcordia's burden to establish that inventorship was proper, substantial evidence introduced at trial nevertheless established that Drs. Lau and Fleisher are the appropriate and only inventors of the SRTS patent:

- Dr. Fleischer explained when and how SRTS was invented. Trial Tr. at 578-79. Dr. Fleischer testified that France Telecom contributed nothing to SRTS and that he and Dr. Lau worked exclusively on SRTS. Trial Tr. at 596, 650-51 (Dr. Fleischer).

---

[10] Despite counsel for Cisco's insistence (even during opening statements before the jury) that Telcordia was using the June 6, 1991, memorandum to establish an earlier conception date, in fact Telcordia presented the June 6, 1991, memorandum to the jury in accordance with the Court's Order on the defendants second motion *in limine*, D.I. 335 at 6-8, and only for the reasons noted in Telcordia's response to the defendants' second motion *in limine*—namely to rebut a narrow aspect of the defendants' derivation theory.

- Mr. Kittams, a former employee who was involved in standards activities at Bellcore and was the interface between Bellcore and France Telecom, testified that SRTS was the sole development of Bellcore:

  Question: Based on your understanding of events as they happened at the time, it's your opinion that SRTS was not the result of cooperative work between France Telecom and Bell but rather was a sole development of Bellcore. Is that right?

  Answer: Based on the events I witnessed, I felt that the technical work on SRTS was done on our side, yes. Trial Tr. 1933 (Mr. Kittams).

- All elements of claims 11 and 33 were included in a paper authored by the inventors Dr. Lau and Fleischer, dated November 4, 1991, which was submitted to the T1S1 committee. PTX-1211; Trial Tr. 587 (Dr. Fleischer).

- Both inventors testified that the August 26, 1991, fax from France Telecom contributed nothing to their work on SRTS. Trial Tr. 598 (Dr. Fleischer); 689, 692, 788-89, 808 (Dr. Lau). The August 26, 1991, fax was understood by the inventors to be discussing the same traditional time stamp that France Telecom proposed and not a new residual time stamp. Trial Tr. 599-600 (Dr. Fleischer), 689, 794-95 (Dr. Lau); *see also* Trial Tr. 1448, 1451-52 (Mr. Adam).

- Dr. Fleischer testified that, after agreeing on the fundamental idea for SRTS with Dr. Lau, he and Dr. Lau worked closely together to "put flesh on the bones" of the idea, putting in "a fair amount of work." Trial Tr. 579, 602 (Dr. Fleischer); *see also* 674, 676 (Dr. Lau).

- On October 11, 1991, Bellcore wrote, for the first time in any exchange between Bellcore and France Telecom, of a "residue-TS" that would be of "2-4 bits." DTX-2369, Trial Tr. 600-01 (Dr. Fleischer); 692-94 (Dr. Lau). But after being informed of SRTS ideas, the engineers at France Telecom counter-proposed "a completely different system" than SRTS. PTX-521; Trial Tr. 605-06 (Dr. Fleischer); 695-96 (Dr. Lau). Bellcore then pointed out the "serious shortcomings" in the latest French proposal and proceeded to provide more detail about SRTS, including the location where the residue-time stamp could be transmitted (in the CI bit of the SAR sublayer, which is outside of the convergence sublayer overhead). PTX-522; Trial Tr. 606-08 (Dr. Fleischer); 697-99 (Dr. Lau); 1681 (Dr. Acampora).

Against this substantial evidence, the jury properly rejected Cisco's improper inventorship theory and properly determined that Cisco failed to establish invalidity of the '633 patent by clear and convincing evidence.

V. The '306 Patent

A. Substantial Evidence Supports the Jury's Determination that the '306 Patent Is Not Invalid

In its JMOL motion, Cisco contends that no reasonable jury could have found that the '306 patent was not invalid. Specifically, Cisco contends that the FasNet and Budrikis references each anticipates the asserted claims of the '306 patent, and alternatively that an unspecified combination of FasNet "and/or" Budrikis and "one or more" of the Turner, Takeuchi, Luderer, or Baran references renders the asserted claims of the '306 patent obvious.[11]

At the outset, Telcordia notes that the '306 patent is presumed to be valid, and Cisco bore the burden at trial of establishing invalidity by clear and convincing evidence. Cisco simply failed to meet its burden, and substantial evidence supports the jury's determination that the '306 patent is not invalid. Specifically, substantial evidence demonstrates, at least, that neither FasNet, Budrikis, nor any of the secondary references that Cisco asserted against the '306 patent, generates frames having an "empty payload field" or writes data into "any available" empty payload field, as required by claims 1, 3, and 4 of the '306 patent.[12]

The "empty payload field" limitation was construed by the Court as "a payload field that is empty of source data, but including bit signals of some kind, i.e., garbage bits." D.I. 179 at ¶ 27. At trial, Cisco's expert provided unclear and contradictory testimony regarding how he

---

[11] Demonstrating the inadequacy with which Cisco presented its invalidity case against the '306 patent, even now—post-trial—Cisco's invalidity contentions remain vague and unclear (*e.g.*, Cisco fails to identify which references, exactly, form the basis of its obviousness contentions).

[12] Cisco suggests that because Telcordia referred only to the "garbage bits" limitation of claims 1, 3 and 4 in its closing argument on '306 validity, Telcordia somehow conceded that all other limitations of the claims are present in the FasNet and Budrikis references. D.I. 376 at 38. Telcordia made no such concession. More importantly, the jury's verdict that Cisco failed to carry its burden of establishing invalidity by clear and convincing evidence could have rested upon Cisco's failure to show any one of the elements of the asserted claims in the prior art—regardless of what Telcordia argued at trial.

used the term "garbage bits" when rendering his opinion. He testified, nearly in the same breath, that "garbage" was "meaningless" and then that the "garbage" wasn't "garbage" or "meaningless" at all, but that "garbage" had to indicate something—emptiness:

> There is no usable data in this slot. It may contain something. That something is what we refer to as being garbage bits. They don't mean anything. They are an indication of the emptiness.

Trial Tr. 1617 (Dr. Acampora). Cisco's expert then further retreated from his requirement that "garbage" is an "indication of emptiness" on cross-examination, testifying that "intentionally placed" bits were not garbage bits if they were "processed somewhere else to accomplish some objective":

> If the bits were intentionally placed with the objective of having them processed somewhere else to accomplish some objective, then they are not garbage bits.

Trial Tr. 1716 (Dr. Acampora). Cross-examination also revealed that FasNet's "empty payload fields" do not contain "garbage bits." Cisco's expert testified that empty payload fields in FasNet must have an all-zero bit pattern. Trial Tr. 1717-18 (Dr. Acampora). Indeed, Dr. Acampora went further and explained that the reason the empty payload fields in FasNet must have an all-zero bit pattern—and cannot tolerate an arbitrary "garbage" pattern—is that the buses in FasNet are "passive lines":

> In a passive bus, how the bus operates is, it's a process know as exclusive or. I don't want to bore you with the details. It basically means, if there is a 1 present in a particular bit location and I want to write a 0, I cannot.

Trial Tr. 1719 (Dr. Acampora). Accordingly, the FasNet system does not have "garbage bits" under Dr. Acampora's definition because FasNet intentionally places all zero bits in empty payload fields with the objective of having them processed [overwritten] somewhere else [at a packet-insertion station] to accomplish some objective [correctly writing packet data into the payload field].

Similarly, the evidence at trial established that the Budrikis system likewise does not have "garbage bits" in the empty payload fields. Budrikis, like FasNet, uses a "passive bus." Trial Tr. 1721 (Dr. Acampora). Indeed, Dr. Acampora explained that packet data can be correctly written into Budrikis' empty payload fields only because the fields contain an all-zero bit pattern:

> They happen to be overwriteable because they are 0's, and the exclusive or allows me to do that.
>
> . . .
>
> If it is a passive bus, then as the empty payload passes the, propagates from the control station, if it is a passive bus then it's got to be all 0's.

Trial Tr. 1720-21 (Dr. Acampora). In essence, due to their passive buses, both FasNet and Budrikis must have a deliberate all 0's pattern—not garbage bits—in their payload fields before data is written into the fields. As such, just like FasNet, the Budrikis system does not have "garbage bits" under Dr. Acampora's definition because Budrikis intentionally places all zero bits in empty payload fields with the objective of having them processed somewhere else to accomplish some objective.

In light of this evidence, the jury's determination that neither FasNet nor Budrikis anticipates the claims of the '306 patent is entirely reasonable and is supported by substantial evidence (i.e., the missing "garbage bits" limitation).

Additionally, both FasNet and Budrikis also fail to disclose the "any available empty payload field" limitation. The terms "available empty payload field" (claims 1 and 3) and "empty payload field of any of said frames available to said inserting means" (claim 4) were construed by the Court as "an empty payload field that can be filled with a data packet from the source, among the plurality of sources, of the highest priority with a data packet ready to

transmit." D.I. 179 at ¶ 35. Moreover, in the language of the '306 claims, each of the above limitations is preceded by the word "any":

- "**any** available empty payload field" (claims 1 and 3);
- "**any** empty payload field of any of said frames available to said inserting means" (claim 4).

Thus, claims 1, 3 and 4 demand that data be written into "any" available empty payload field, i.e., any payload field can be filled with a data packet from the source of highest priority with a packet ready to transmit.

Cisco's expert initially explained to the jury that the system of the '306 patent has a priority scheme based on the position of the framers on the bus. He testified that the framer that is closest to the head end of the bus and has a packet ready to transmit always sends the packet in the next empty payload field ("slot"). Trial Tr. 1628 (Dr. Acampora). In the '306 patent, Cisco's expert explained, the next empty payload field is always available to receive the packet that is of the highest priority ready to transmit (that is, no empty payload field passes by a waiting packet). Trial Tr. 1713-14 (Dr. Acampora).

In contrast, Cisco's expert described the FasNet reference as having a priority scheme that cycles, creating a "lockout period":

> If you have a lot of information to send, you are going to fill each and every time slot. The people to the right are not going to be too happy. They have stuff to send also and they are just going to see a continuous sequence of filled time slots.
>
> What the FasNet authors imagined was a scheme that would prevent that. So they declared a notion of a cycle. And if you have already written in that cycle, you automatically become low priority for the remainder of that cycle. You cannot write twice in one cycle.
>
> If I am at the head end, and I see the start of a new cycle, and I have a packet ready to go, I see an empty slot, I write my packet into the empty slot.

> I have another packet that is ready to go. I see the next empty slot, I cannot send. The rules of access tell me, no, you can only send once per cycle. Until you have been told another cycle is about to start, you cannot -- the end result is the slot you would have seized is now available for somebody to your right.
>
> That is the whole objective. The access scheme in FasNet is a dynamic priority scheme whereby once you have written for a certain lockout period, you cannot write a second time. You automatically become low priority.

Trial Tr. 1612-1613 (Dr. Acampora). The lockout period of FasNet is significant because, as explained by Dr. Acampora (and in contrast with the '306 patent), when a station has a packet ready for transmission but is locked-out, the station cannot insert its packet into an empty payload field even if no other stations have a packet ready for transmission (that is, that an empty payload field will pass by a waiting, highest priority packet):

> Since you raised it, suppose an empty slot finds its way to the end of the bus. At that point, at the end of the bus, a signal will be sent back on the return bus, not the bus you were contending for, but on the return bus indicating that an empty packet found its way all the way down the bus. That means at least for one frame, everyone passed.
>
> In fact, the tail-end of the station now sends a signal using the return bus to the head end station saying it's time to start a new cycle.

Trial Tr. 1711 (Dr. Acampora). Moreover, Cisco's expert testified that the priority scheme of Budrikis works the same way as the FasNet reference for the purposes of his validity analysis. Trial Tr. 1714 (Dr. Acampora). As such, due to the operation of their priority schemes, neither FasNet nor Budrikis meets the requirement of inserting packets into "any" available empty payload field as there are times when empty payload fields cannot accept the packet of a highest priority ready to transmit. Again, against this testimony, substantial evidence supports the jury's determination that the '306 patent is not invalid because the prior art does not disclose the "any available empty payload field" limitation.

Finally, Cisco failed to introduce any evidence demonstrating that a secondary reference (*i.e.*, Turner, Takeuchi, Luderer, or Baran) somehow remedies the deficiencies of FasNet or Budrikis. In other words, even assuming that these references could be properly combined with FasNet or Budrikis (and assuming that Cisco actually disclosed which references should be combined, and how and why the should be combined), there is no testimony that the "garbage bits" or "any available empty payload field" limitations are disclosed in Turner, Takeuchi, Luderer, or Baran. As such, the jury's determination that the '306 patent is not invalid remains reasonable on multiple grounds and supported by substantial evidence.

B. Cisco's Footnote Motion for a New Trial On Invalidity and Unenforceability of the '306 Patent Should Be Denied

Cisco contends that it should be given a chance for a new trial on invalidity and unenforceability of the '306 patent, hedging against reversal of this Court's claim construction ruling regarding the '306 patent. D.I. 376 at 40 n.16. Cisco's request is a premature and inappropriate request for an advisory opinion. The question of how, if at all, any further proceedings will be governed on remand is entirely hypothetical and, in any event, would be dependent upon exactly how the Federal Circuit might rule.

VI. Conclusion

For the reasons stated above, Telcordia respectfully requests that the Court deny Cisco's motions for JMOL.

ASHBY & GEDDES

/s/ *Steven J. Balick*

Steven J. Balick (I.D. #2114)
John G. Day (I.D. #2403)
Tiffany Geyer Lydon (I.D. #3950)
500 Delaware Avenue, 8th Floor
P.O. Box 1150
Wilmington, DE 19899
(302) 654-1888

Attorneys for Plaintiff
Telcordia Technologies, Inc.

Of Counsel:

Donald R. Dunner
Steven M. Anzalone
Richard H. Smith
Vincent P. Kovalick
Laura P. Masurovsky
James T. Wilson
John M. Williamson
FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.
901 New York Ave., N.W.
Washington, D.C. 20001
(202) 408-4000

Dated: July 23, 2007
182527.1